CLAIMS

WHAT IS CLAIMED IS:

1. A land grid array (LGA) carrier, comprising:

an interposer having a first surface and a second surface opposite the first surface,

a plurality of locations on the first surface adapted to receive a plurality of semiconductor dice and passive components; and

a plurality of conductive pads coupled to the second surface and electrically coupled with selected ones of the semiconductor dice and passive components.

2. The LGA carrier of claim 1 further comprising a plurality of solder balls, wherein at least some of the conductive pads have one of the solder balls attached thereto.

3. The LGA carrier of claim 1 further comprising a plurality of pins, wherein at least some of the conductive pads have one of the pins attached thereto.

4. The LGA carrier of claim 1, wherein the interposer is fabricated out of an organic material.

5. The LGA carrier of claim 1 further comprising a plurality of conductive traces in the interposer arranged to electrically couple the locations in a predefined manner, the conductive traces further electrically coupled to at least some of the conductive pads.

6. The LGA carrier of claim 5 wherein at least some of the conductive pads do not have conductive traces electrically coupled thereto.

7. The LGA carrier of claim 1, wherein the conductive pads are configured in an array of rows and columns.

8. The LGA carrier of claim 7 wherein the array comprises at least 40 rows and at least 45 columns.

9. The LGA carrier of claim 8 wherein the plurality of conductive pads comprises at least 1,800 conductive pads.

10. The LGA carrier of claim 8 wherein the array of conductive pads covers essentially the entire second surface.

11. The LGA carrier of claim 1 wherein the first surface comprises first and second portions, wherein the first portion is adapted to receive the plurality of semiconductor dice and passive components.

12. The LGA carrier of claim 11 wherein the second portion is located about the periphery of the first surface, generally surrounding the first portion.

13. The LGA carrier of claim 12 wherein the second portion is not adapted to receive the semiconductor dice.

14. The LGA carrier of claim 1 further comprising a plurality of semiconductor dice coupled to the first surface.

15. The LGA carrier of 14 wherein the plurality of semiconductor dice comprise memory chips.

16. The LGA carrier of claim 14 wherein the plurality of semiconductor dice are coupled to the first portion using controlled collapse chip connection (C4).

17. The LGA carrier of claim 14 further comprising a plurality of passive components coupled to the first surface.

18. The LGA carrier of claim 17 wherein the plurality of passive components comprise inductors, resistors and capacitors.

Sub A2 > 19. A method of assembling a multi-chip device comprising the acts of:

fabricating an interposer having a first surface and a second surface;

populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of predefined conductive pads; and

coupling at least one of semiconductor dice and a plurality of passive devices to the first surface.

20. The method of claim 19 further comprising the act of coupling the interposer to a substrate.

21. The method of claim 19 wherein the fabricating act comprises fabricating the interposer out of an organic material.

22. The method of claim 19 wherein the second coupling act comprises C4.

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23. The method of claim 19 further comprising the act of testing the semiconductor dice coupled to the interposer prior to the coupling the interposer to the substrate act.

24. The method of claim 19 further comprising the act of coupling a single chip carrier to the substrate.

25. The method of claim 19 wherein the second coupling act comprises coupling memory chips to the interposer.

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